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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,717	06/25/2001	Jerrell Hein	026-0006	8760

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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,717	HEIN ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,24 and 25* is/are rejected.

7)☒ Claim(s) *20-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *041502*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The application appears to have provisional priority data of 03/26/2001 from application no. 60/278,784. Please include a continuation data in the first sentence of the specification.

Drawings

2. Figures 1A ~ 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-14,17 and 19-23 are objected to because of the following informalities:

In claim 1, line 10, delete "signal the" and insert "signal by delaying the".

In claim 7, line 3, delete "clock." and insert "clock signal.".

In claim 8, line 2, delete "first and" and insert "first register and".

In claim 8, line 3, delete "receive data" and insert "receive retimed data".

In claim 8, line 4, delete "clock and" and insert "clock signal and".

In claim 8, line 7, delete "clock and to receive data" and insert "clock signal and to receive the retimed data".

In claim 8, line 9, delete "register data retimed" and insert "register of the retimed data".

In claim 8, line 10, delete "clock." and insert "clock signal.".

In claim 9, line 2, delete "last register" and insert "last registers".

In claim 9, line 3, delete "plurality of registers" and insert "plurality of serially coupled registers".

In claim 9, line 3, delete "clock." and insert "clock signal.".

In claim 13, line 2, delete "write data" and insert "write retimed data".

In claim 17, line 1, delete "as recited in claim 15".

In claim 19, line 4, delete "clock." and insert "clock signal.".

In claim 20, lines 3 and 10, respectively, delete "data" and insert "the input data".

In claim 20, line 8, delete "the successively" and insert "the plurality of successively".

In claim 20, line 10, delete "clock to" and insert "clock signal to".

In claim 22, lines 2 and 3, delete "data" and insert "the input data".

In claim 22, line 3, delete "retime data" and insert "retime the input data".

In claim 22, line 3, delete "clock to" and insert "clock signal to".

Claims 2-6,10-12,14,21 and 23 directly or indirectly depend on claim 1,20 or 22.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 2,8 and 10, respectively, recite "...coupled to...". However, it is unclear and indefinite as to which element is coupled to.

In claims 2,3, lines 2,2, respectively, recite "...coupled to...". However, it is unclear and indefinite as to which element it is coupled to.

In claim 8, lines 3,4 and 9, respectively, recite "...coupled to...". However, it is unclear and indefinite as to which element it is coupled to.

Claims 4-7 and 9-14 directly or indirectly depend on claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4,6,7,11,15-17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea, USP 6,542,040 B1 in view of Applicants' Admitted Prior Art (AAPA).

Regarding claims 1,15 and 24, Lesea discloses a clock recovery circuit (see Fig.2) comprising: a phase detector circuit (101,103) coupled to generate a difference signal (PHOUT, DIGITAL OUT) indicating a phase difference between an incoming signal (SIN) and a clock signal (SOSC); an oscillator circuit (106, further illustrated in Fig.7) responsive to a control signal (SUPPLY) derived from the difference signal (PHOUT) to generate an output clock signal (output of 507 in Fig.7) variable according to the control signal (SUPPLY). Lesea further teaches a clock delay circuit (508 and 503 in Fig.7) coupled to receive a delay control signal derived (BIN or DIGITAL OUT) from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal (SOSC) the output clock signal delayed according to the delay control signal. Although Lesea teaches applying phase detection between a clock and an incoming signal, Lesea does not explicitly teach wherein the incoming signal (SIN) is an incoming data stream. AAPA teaches a phase detector (102 in Fig.1A) detecting a phase difference between the clock signal (CLOCK) and the incoming data stream (104). Therefore, it would have been obvious to one skilled in the art at the time of the invention to apply the incoming

data stream taught by AAPA as the incoming signal (SIN) of Lesea for the purpose of applying a clock recovery of the incoming data signal. (note col.3, line 50 – col.4, line 41 and col.8, line 19 – col.9, line 37)

Regarding claims 2,4 and 17, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1 or 15. Although Lesea does not explicitly teach a loop filter circuit, AAPA further teaches applying a loop filter circuit (112 in Fig.1A) to receive the difference signal (116) and supply a filtered output as the control signal. Therefore, it would have been obvious to one skilled in the art at the time of the invention to apply the loop filter circuit between the phase detector (101 and 103 in Fig.2) and the oscillator (106) for the purpose of filtering out any unwanted signal components of the difference signal (PHOUT and DIGITAL OUT). Thus, having a delay control filter circuit (112 in Fig.1A) to receive the difference signal (PHOUT, DIGITAL OUT) and generate the delay control signal (DIGITAL OUT input to 503 in Fig.7) based thereon.

Regarding claims 3 and 16, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1 or 15. Lesea further teaches wherein the control signal (SUPPLY) derived from the difference signal (PHOUT, DIGITAL OUT) for the oscillator circuit is used as the delay control signal, also derived from the difference signal (DIGITAL OUT, controlling 503 in Fig.7).

Regarding claims 6 and 7, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1. Lesea further teaches wherein the clock delay circuit comprises multiple stages. (see 700-706 in Fig.9 having flip-flops creating multiple stages, and note col.11, lines 12-31) And further, Lesea teaches wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal through DIV2, DIV32 AND DIV256.

Regarding claim 11, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1. Lesea further teaches wherein the oscillator circuit is a voltage controlled oscillator. (106 in Fig.2 and further 507 in Fig.7, wherein it is controlled by SUPPLY, control voltage, note col.9, lines 23-37)

6. Claims 10,12,18,19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea, USP 6,542,040 B1 in view of Applicants' Admitted Prior Art (AAPA) and Akashi, USP 6,178,212 B1.

Regarding claims 10,12,18 and 25, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1,15 or 24. As explained previously, Lesea in view of AAPA teach phase detecting between the input data stream and the delayed clock signal. However, Lesea in view of AAPA do not explicitly teach a data recovery circuit. Akashi teaches phase detector (21,22,24 in Fig.1) coupled to a data recovery circuit or means for retiming the incoming data signal (28)

from the delayed clock signal (Cref, which is inputted to the phase detector). Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify Lesea's system by coupling the data recovery circuit, taught by Akashi, to the phase detector (101 in Fig.2) of Lesea for the purpose of properly recovering the incoming data stream. Thus, retime the incoming data signal from the delayed clock signal to the output clock signal (output of 507 in Fig.7) where the difference signal adjusts the output clock signal.

Regarding claim 19, Lesea in view of AAPA and Akashi teach all subject matter claimed, as applied to claim 18. Lesea further teaches wherein the clock delay circuit comprises multiple stages. (see 700-706 in Fig.9 having flip-flops creating multiple stages, and note col.11, lines 12-31) And further, Lesea teaches wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal through DIV2, DIV32 AND DIV256.

7. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea, USP 6,542,040 B1 in view of Applicants' Admitted Prior Art (AAPA) and Bulzachelli (cited in the IDS).

Regarding claim 5, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1. Lesea, as previously explained, teaches the clock delay circuit (108 and 503 in Fig.7), but does not teach the clock delay circuit is a voltage

controlled delay circuit. Bulzachelli teaches the clock delay circuit is a voltage controlled delay circuit (see 418 in Fig.4). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to analyze that the clock delay circuit taught by Lesea and Bulzachelli perform equal function. Applicant has not disclosed that voltage controlled delay circuit provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the clock delay circuit taught by Lesea because Lesea's system provides a programmable delay-line with an efficient calculation through the use of non-inverting buffers with propagation delay of approximately 100 picoseconds. (note col.8, lines 42-49) Therefore, it would have been obvious to combine to one of ordinary skill in this art to modify Lesea's clock delay circuit with Bulzachelli's receiving control voltage to obtain the invention as specified in claim 5.

Regarding claim 14, Lesea in view of AAPA teach all subject matter claimed, as applied to claim 1. As explained previously, AAPA teaches a loop amplifier and filter (112) coupled to the phase detector (102) having a closed loop response (as illustrated in Fig.2 of Lesea and in Fig.1A of AAPA. However, Lesea in view of AAPA do not explicitly teach having the closed loop response without an explicit zero. Bulzachelli also teaches a phase detector (see 102 and 202 in Figs. 1 and 2) having a closed loop response and further teaches the loop amplifier

and filter having an integrator plus other circuitry and contains an explicit zero. Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify AAPA's loop amplifier and filter (112) to incorporate the integrator and other circuitry to provide an explicit zero for the purpose of providing a loop stability, as taught by Bulzachelli. (note col.3, lines 20-32)

Allowable Subject Matter

8. Claims 8 and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims, and overcome the claim objections.

9. Claims 20-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and overcome the claim objections.

10. The following is a statement of reasons for the indication of allowable subject matter: Present application discloses a phase locked loop comprising a phase detector, oscillator and a clock delay circuit, wherein the clock delay circuit is configured to receive output signal from the oscillator and derived version of a difference signal, which is generated by the phase detector. Closest prior art, Lesea in view of AAPA, teach all subject matter claimed. However, prior art do not teach or suggest, solely or in combination, a data recovery circuit coupled to the phase detector having FIFO memory or registers wherein the data recovery circuit is retimed by writing the data

synchronized to the delayed clock signal and reading the data from the memory with the output clock. And further, prior art do not teach a plurality of successively coupled registers providing different delayed clock signals, as recited in claims 8 and 20. Therefore, prior art do not teach all the limitations claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
10/29/04

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PRIMARY EXAMINER